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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/743,073

12/23/2003

Takashi Ichimori

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03/02/2005

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EXAMINER

MONDT, JOHANNES P

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No. 10/743,073	Applicant(s) ICHIMORI, TAKASHI	
	Examiner Johannes P. Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 December 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 14-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/23/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of the Group I invention drawn to a method of making a ferroelectric device, claims 1-13, in the reply filed on 12/29/2004 is acknowledged.

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement filed 12/23/2003. A signed copy of Form PTO-1449 is enclosed with this office action.

Specification

2. *The Specification is objected* to because of the following informalities: the "insulating substrate" of claim 1 (and claims dependent therein) has not been specifically disclosed in the Specification. Although said "insulating substrate" is in the original claims and thus does not constitute new matter, the Specification has to include disclosure of a substrate that is insulating. The only substrate disclosed in the Specification is a "semiconductor substrate" (referred to by numeral 1 on page 7, line 5). Said semiconducting substrate may or may not be insulating dependent upon its conductivity type and doping concentration. A statement that said semiconductor substrate performs an insulating function would suffice. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 4-7** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, an etching step inherently consists of an etching process, and does not include a process of film or layer formation. Yet, according to claim 4 a first cover film is formed in an etching step. This renders the claim indefinite.

5. **Claim 5** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, while by dependency on claim 4 said first cover film is formed in said second etching step, claim 5 claims said first cover film is etched in said second etching step. This renders the claim indefinite.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 1, 4, 8, 9, 10, 12 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al (US 2002/0074601 A1) in view of the Prior Art as Admitted by Applicant, or, in the alternative, in view of Kanaya et al (6,611,014 B1). *Fox et al teach a method of manufacturing a ferroelectric device* (see title) comprising steps of:

providing an insulating substrate 100 (par. [0039]);

forming a multi-layer body depositing successively a contact film 102 ([0038]), a lower electrode 104 ([0039]), a ferroelectric film 106/108 ([0040]) and an upper electrode 110 ([0044]) on said insulating substrate; and etching said multi-layer body (steps 300 and 404; see Figure 4 and [0053]-[0056]) including:

a first etch step 300 for etching said upper electrode and said ferroelectric film (Figure 4 and [0053]);

a heat treatment step 402 (Figure 4 and [0055]; see also the equivalent step 208 as described in [0041]) for heat-treating said ferroelectric film under a condition wherein said contact film is covered with said lower electrode; and

a second etching step 404 (Figure 4 and [0056]) for etching said lower electrode.

Fox et al do not necessarily teach the further limitation that said second etching step also etches said contact film 102, thereby exposing said insulating substrate 100.

However, it would have been obvious to include said further limitation in view of Prior

Art as Admitted by Applicant, or, in the alternative, in view of Kanaya et al: said Prior

Art as Admitted by Applicant teaches that the second etching step etches not only the

lower electrode but also the contact film (see page 3; and see page 4 for the definition

of contact film to include any binding film); with regard to the alternative rejection,

Kanaya et al teach the second step to etch the contact film 301 (col. 8, l. 42-58 and col.

11, l. 60-64: it is noted that the hydrogen barrier layer, be it 101 or 301, is an adhesive

layer and thus meets the definition of contact layer in the Specification, page 4).

Motivation to include the teaching by the Prior Art as Admitted by Applicant, or, in the

alternative, the teaching by Kanaya et al, at least derives from the function of said contact layer, as a layer to make contact with the lower electrode: in the locations where said lower electrode is absent there also is no need for said contact layer. Thus a more functionally focused device is achieved.

On claim 4: this rejection is provided subject to the noted indefiniteness (see rejection under 35 U.S.C. 112, 2nd paragraph, of claims 4-7 above) to the best of examiner's understanding. Said second etching step 404 by Fox et al includes forming a first cover film (masking film) so as to cover said upper electrode, ferroelectric film and lower electrode and etching said first cover film together with said multi-layer body (Figure 4 and [0056]).

On claim 8: the method by Fox et al further comprises a step 218 for forming a second cover film 112 ([0049] and [0056] and Figure 4) so as to cover said multi-layer body after said second etching step.

On claim 9: the method by Fox et al further comprises an additional heat treatment step 406 ([0056] and Figure 4) for heat-treating said ferroelectric film after said second cover film forming step.

On claim 10: the contact film 102 of the method by Fox et al includes a binding film 102 ([0038] and Figure 4).

On claim 12: said heat treatment in Fox et al is performed to recover a crystalline structure in the ferroelectric film ([0041], [0051] and [0055]).

On claim 13: said additional heat treatment in Fox et al and as claimed here in claim 9 is performed to recover a crystalline structure in the ferroelectric film ([0016];

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see the patent cited and incorporated by reference in Fox et al in this regard), while furthermore the additional heat treatment (anneal) inherently causes further crystallization unless crystallization is perfect to start with.

8. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al and either Prior Art as Admitted by Applicant or, in the alternative, over Fox et al and Kanaya et al as applied to claim 1 above, and further in view of Jung et al (JP 2001-044377, IDS item AJ). *Fox et al teach* said insulating film 100 formed on a semiconductor substrate having a transistor ([0038]) (i.e., "CMOS integrated circuit wafer"). *Fox et al do not necessarily teach* the further limitation that a contact plug to be formed so as to pass through said insulating layer film and electrically connecting said transistor to said contact film. However, it would have been obvious to include said further limitation in view of Jung et al, who, in a patent publication on a ferroelectric capacitor for a transistor, hence analogous art, teach a contact plug 114 formed so as to pass through said insulating film 108/112 and electrically connect the transistor (with gate 104 and source/drain regions 106) with said contact film (through its un-etched sides). *Motivation* to include the teaching in this regard by Jung et al in the invention by Fox et al derives from the obvious applicability of the invention by Fox to those FRAM embodiments wherein the electrical connection between the drain region of the transistors of the CMOS integrated circuit and the ferroelectric capacitor is achieved through the insulating substrate over the CMOS wafer, i.e., through the shortest route possible, thus saving ohmic dissipation and material investment.

9. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al in view of Prior Art as Admitted by Applicant. As detailed above, claim 1 is unpatentable inter alia over Fox et al in view of Prior Art as Admitted by Applicant. Furthermore, in the first etching step in the Prior Art as Admitted by Applicant the lower electrode is partly etched in the first etching step so as to arrive at a predetermined thickness of the lower electrode. *Motivation* to include the teaching in this regard by Prior Art as Admitted by Applicant at least derives from the implied means to set the thickness of the lower electrode.

10. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al and Prior Art as Admitted by Applicant, or, in the alternative, over Fox et al and Kanaya et al as applied to claim 10 above, and further in view of Nagano et al (US 2002/0195633 A1). As detailed above claim 10 is unpatentable over Fox et al in view of either Prior Art as Admitted by Applicant or Kanaya et al. Neither Fox et al, nor Prior Art as Admitted by Applicant, - nor Kanaya et al, necessarily teach the further limitation of the contact film to include an oxidation barrier film. However, it would have been obvious to include said further limitation in view of Nagano et al, who, in a patent on a ferroelectric capacitor for a semiconductor memory device (title, abstract, [0004], [0104]), - hence analogous art, teach the inclusion of an iridium oxide (IrO_2) oxygen barrier film 31, as well as an iridium (Ir) oxygen barrier film between a platinum (Pt) lower electrode and the substrate so as to prevent the cross-layer diffusion of oxygen (Figure 1B, abstract, [0013] and [0103]). *Motivation* to include the teaching in this regard by Nagano et al in the invention by Fox et al derives from the deleterious effect of

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oxygen diffusion to contact plugs in ferroelectric capacitor semiconductor devices. The teaching can be *combined* with the invention because the material constitution of the layers (oxide substrate 45 ([0179]), platinum lower electrode 31d ([0103]) and lead zirconate titanate (PZT) (inter alia) ([0185]) and the generally metallic constitution of the contact plug to be protected against oxidation, imply the same conditions for oxygen diffusion, thus requiring the same measures.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Eastep (6,090,443) (incorporated by reference into Fox et al as cited); Kasko et al (US 2002/0137301 A1); Kasko et al (6,613,640 B2); Zhang et al (US 2002/0135067 A1); Zhang et al (6,566,753 B2); Zhang et al (6,479,304 B1); Zhang et al (6,399,521 B1); and Ohyagi (US 2003/0211685 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
March 1, 2005

Patent Examiner:

A handwritten signature in black ink, appearing to read 'J. Mondt', with a stylized flourish at the end.

Johannes Mondt (Art Unit: 2826).